

### DETAILED ACTION

This is a response to the RCE filed 10/25/2011. Claims 26-28 are pending and are under examination.

#### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Toyoshima et al. (USP 6,271,687) in view of Branson et al. (USP 5,508,644).

Regarding claim 26, figure 3 of Toyoshima et al. shows an apparatus comprising a first supply rail (Vcc), second supply rail (GND), first output terminal (STT02), second output terminal (STB02), first PMOS transistor (MP204), second PMOS (MP205), first NMOS (MN201), second NMOS (MN202), clocking circuit (MP201, MP202, MP203, MP208), third NMOS (MN203), fourth NMOS (MN204), differential signals (CDB02, CDT02), fifth NMOS (M205), precharge circuit (MP206, MP207).

The difference seen between Toyoshima et al. and the present invention are: (1) the sixth transistor and its connection; (2) a RS flip flop receiving output signals from the output terminals as called for in claims 26-28.

Branson et al.'s figure 1 shows a sense amplifier including the transistor 26 coupled to the differential transistor pairs (20, 22) and the ground terminal. Transistor 26 is used to sink the current from transistors 20-22 to ground terminal to reduce power dissipation thus preventing

erroneous operation. Therefore, it would have been obvious to person skilled in the art at the time the invention was made to include the Branson et al.'s transistor 26 in the circuit arrangement of Toyoshima et al.'s figure 3 for the purpose of reducing power dissipation thus preventing erroneous operation.

Regarding an RS flip flop coupled to the output terminals of Toyoshima et al., the circuit arrangement of Toyoshima et al.'s is capable of having the output terminals STT02 and STB02 coupled to the input terminals of the RS flip flop. Outside of any non-obvious results, the obviousness of having the RS flip flop receives output signals of Toyoshima et al.'s figure 3 will not be patentable under 35USC 103(a).

3. Claims 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barnes (USP 2003/0052715) in view of Branson et al. (USP 5,508,644).

Regarding claim 26, figure 5 of Barnes shows an apparatus comprising a first supply rail (Vdd), second supply rail (GND), RS flip flop (SRlatch, figure 3), first output terminal (114), second output terminal (116), first PMOS transistor (T1), second PMOS (T2), first NMOS (T4), second NMOS (T3), clocking circuit (T8, T9), third NMOS (T6), input signal (Vin), fourth NMOS (T7), a reference signal (Vref), fifth NMOS (T12), precharge circuit (T10, T11).

The difference seen between Barnes reference and the present invention are: (1) the sixth transistor and its connection; (2) the input signals are Vin and Vref instead of differential input signals as called for in claim 26.

Branson et al.'s figure 1 shows a sense amplifier including the transistor 26 coupled to the differential transistor pairs (20, 22) and the ground terminal. Transistor 26 is used to sink the

current from transistors 20-22 to ground terminal to reduce power dissipation thus preventing erroneous operation. Therefore, it would have been obvious to person skilled in the art at the time the invention was made to include the Branson et al.'s transistor 26 in the circuit arrangement of Barnes' figure 5 for the purpose of reducing power dissipation thus preventing erroneous operation.

Regarding the input signals to be differential signals as called for in claim 26, one skilled in the art should have recognized that the Barnes' sensing amplifier performance will not change with differential input signals. Therefore, outside of any non-obvious results, the obviousness of having Barnes' sense amplifier receive differential input signals will not be patentable under 35USC 103(a).

4. Claims 27-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barnes (US 2003/0052715) and Branson et al. (USP 5,508,644) as applied to claim 26 above, and further in view of Kanamori et al. (US 2002/0171453).

The combination of Barnes and Branson et al. reference shows all the aspects of the present invention, as noted above, except for the fifth PMOS transistor and sixth PMOS transistor (i.e., transistors 32 and 34 of the present invention's figure 1) as called for in claim 27.

Figure 5 of Kanamori et al. shows a sense amplifier including equalizing transistors 160 and 140 perform voltage equalization between two nodes in order to preventing erroneous operation. Therefore, it would have been obvious to person skilled in the art at the time the invention was made to include Kanamori et al.'s equalizing transistors 160 and 140 in the circuit arrangement of Barnes to perform voltage equalization between nodes for the purpose of minimizing erroneous operation.

Regarding claim 28, the precharge seventh and eighth PMOS transistors are seen as the transistors T8 and T9 of Barnes's figure 5.

5. Claims 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanamori et al. (US 2002/0171453) in view of Branson et al. (USP 5,508,644) and Toyoshima et al. (USP 5,854,562).

Regarding claim 26, figure 5 of Kanamori et al. shows an apparatus comprising a first supply rail (AVD), second supply rail (AVS), first output terminal (q), second output terminal (qx), first PMOS transistor (111), second PMOS (121), first NMOS (112), second NMOS (122), clocking circuit (110, 120, 160, 140), third NMOS (101), fourth NMOS (102), differential signals (d, dx), fifth NMOS (130), a RS flip flop receiving output signals from the output terminals (figure 18).

The difference seen between Kanamori et al. and the present invention are: (1) the sixth transistor and its connection; (2) precharge circuit as called for in claims 26-28.

Branson et al.'s figure 1 shows a sense amplifier including the transistor 26 coupled to the differential transistor pairs (20, 22) and the ground terminal. Transistor 26 is used to sink the current from transistors 20-22 to ground terminal to reduce power dissipation thus preventing erroneous operation. Therefore, it would have been obvious to person skilled in the art at the time the invention was made to include the Branson et al.'s transistor 26 in the circuit arrangement of Kanamori et al.'s figure 5 for the purpose of reducing power dissipation thus preventing erroneous operation.

Regarding the precharge circuit including the seventh PMOS transistors and eighth PMOS transistors (transistors 20 and 30 of the present invention's figure 1), figure 3 of

Toyoshima et al. reference shows a sense amplifier including precharging transistors MP206 and MP207 perform precharging the drain electrodes of the transistors MN203 and MN204 to a predetermined voltage to prevent erroneous operation. Therefore, it would have been obvious to person skilled in the art at the time the invention was made to include the Toyoshima et al.'s precharging transistors (MP206 and MP207) in the circuit arrangement of Kanamori et al.'s figure 5 for the purpose of precharging the drain electrodes of the transistors 101 and 102 to a predetermined state thus to prevent erroneous operation.

### *Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to TUAN T. LAM whose telephone number is (571)272-1744. The examiner can normally be reached on Monday to Friday (7:30 am to 6:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lincoln Donovan can be reached on 571-272-1988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/TUAN T LAM/  
Primary Examiner, Art Unit 2816

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